A 2 GHz SUBHARMONIC SAMPLER FOR SIGNAL DOWNCONVERSION

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ABSTRACT

Subharmonic sampling is a discrete-time alternative for the signal downconversion problem. It can be used either to replace a traditional continuous-time mixer in a superheterodyne receiver or can be combined with other discrete-time analog signal processing blocks in novel receiver architectures. We present a 2 GHz bandwidth integrated mixer based on subharmonic sampling. The sampler uses a two-diode topology with a 3V supply. The downconversion loss for the passive sampler is 1 dB and the total system gain 3 dB. The mixer achieves IIP3 of +16 dBm and -1dB compression +7 dBm for a single-tone input.

INTRODUCTION

In the sampling process, harmonic components, generated in the switching operation, mix with the band-limited input signal and produce replicas over a wide range of frequencies. A replica, located at baseband or close to it, can be used as a downconverted signal in baseband or IF signal processing [1]. Therefore, in comparison to classical continuous-time mixers, an additional degree of freedom for LO frequency selection is available. To prevent aliasing of signal replicas, a sampling frequency at least twice the signal bandwidth must be chosen. By appropriate choice of the switch duty cycle a small conversion loss for a passive structure can be achieved.

To produce the desired IF frequency we can choose from the set of sampling frequencies given by the equation $f_{IF}=\min(|f_{RF}-nf_{LO}|)$, where n is an integer called the sampling ratio. In Fig. 1 two different sampling frequencies produce the same IF. The higher sampling frequency produces less harmonic components close to the desired IF. The more significant benefit for using a high sampling frequency comes from the fact that every switching harmonic converts noise around it to baseband. Because one source of the noise is the switch resistance of the sampler, the internal noise aliasing problem can only be reduced by increasing the sampling frequency thus giving a 3 dB benefit per octave.

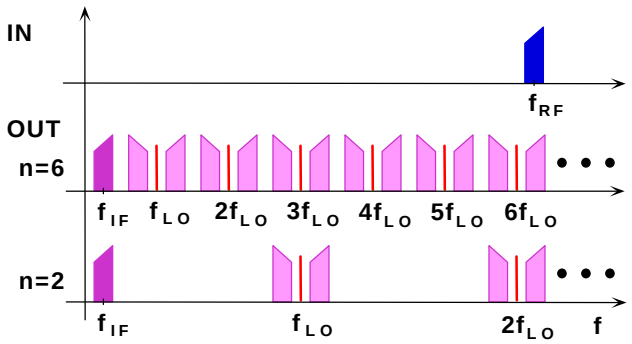

Fig. 1. Spectral behavior of a subharmonic sampler with two different sampling ratios

In this paper, we demonstrate for the first time a fully integrated subharmonic mixer with an on-chip strobe pulse generation circuit capable of handling input signals up to 2 GHz with small conversion loss and high third-order intercept and compression

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points. It uses a pair of two-diode bridges and operates with a single 3V power supply, which is very low for a diode bridge sampler. Our approach uses a relatively high sampling frequency to reduce the noise aliasing problem inherent in subharmonic samplers. Some earlier subharmonic samplers for RF-mixing are limited to use sampling frequencies close to twice the signal bandwidth because of circuit topology constraints [2],[3],[4]. Our circuit can operate at sampling frequencies up to 1.5 GHz, which is significantly larger than the typical input signal bandwidth of a mobile receiver.

CIRCUIT DESCRIPTION

The circuit consists of the sampling circuit, an output buffer, and the strobe pulse generation circuit. Fig. 2 shows the block diagram of the downconverter. The differential high frequency input signal is divided to two separate single-ended samplers which have common differential buffer in the output. The strobe pulses are generated on-chip from an external signal source. Two sampling bridges are used because even a slight asymmetry between the positive and negative pulses would limit the dynamic range at low input signal levels in case of a single sampler.

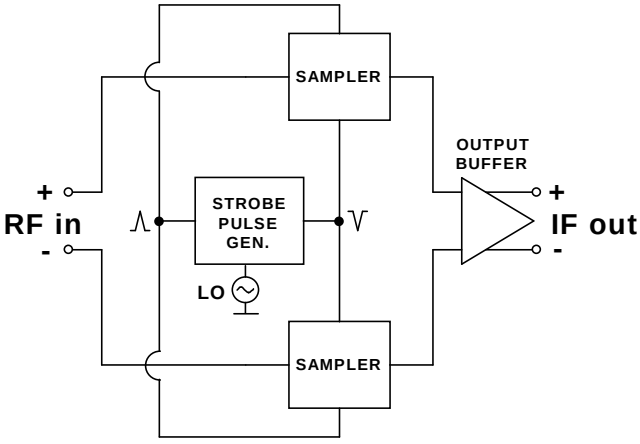

Fig. 2. Block diagram of the circuit. Differential input and output signals are combined after DC isolation by using discrete 180° hybrids in the measurement set-up.

Sampling Bridge

The two-diode bridge [6] in Fig. 3 is capable of operating with a low supply voltage because the strobe pulse circuit can be DC decoupled. The diodes conduct when the sharp strobe pulses pull the voltage over the turn-on point. The current from the pulse generator charges the hold capacitor to a voltage proportional to the input. The falling edge of the strobe turns off the diodes and switches the sampler to hold mode. In the hold mode, the hold capacitor connected to a high impedance buffer keeps its value with a small droop. Simultaneously, the coupling capacitors discharge through the bridge resistors because the output node of the bridge is at a virtual ground for the strobe circuit. The resistors also keep the voltage at the top and bottom of the bridge equal to the output during the hold mode, and therefore no bootstrap diodes are needed.

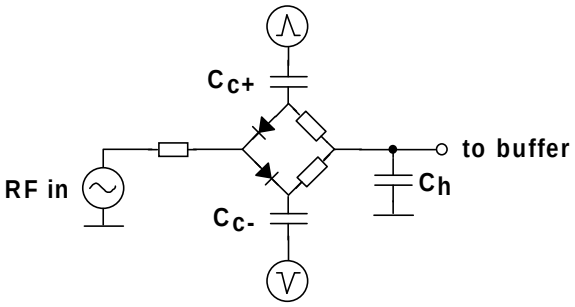

Fig. 3. Two-diode sampling bridge. The hold and coupling capacitance values are all 0.5 pF.

Output Buffer

A high impedance buffer is needed to minimize the droop during the hold mode. We used a differential common source amplifier with resistive loads followed by two emitter followers driving the 50Ω loads in the measurements. The simulated buffer gain is 4 dB and the input transistors are biased through the sampling bridges.

Strobe Pulse Circuit

The sampling pulses are generated by an SCFL differential delay chain coupled to an OR gate as shown in Fig. 4 [7]. A sinusoidal LO input of

approximately 0 dBm is amplified, and the delayed edges of the LO produce positive and negative sampling pulses as illustrated in the timing diagram. A sampling pulse width of approximately 350 ps was determined by simulations and was sufficient to achieve full charge on the hold capacitor in all cases.

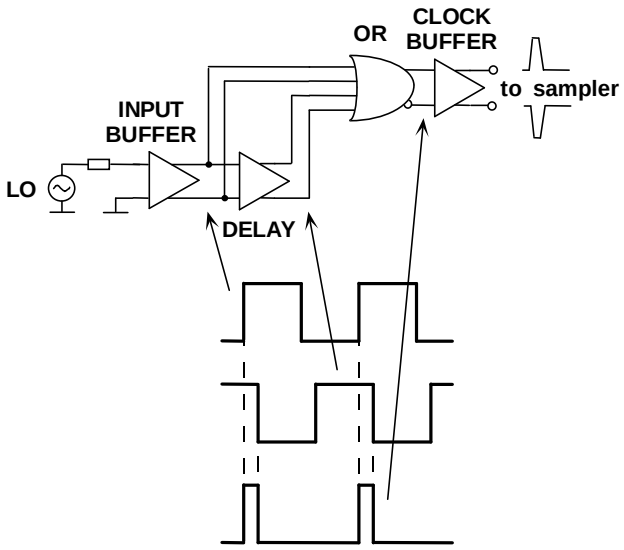

Fig. 4. Strobe pulse generator circuit with timing diagram

The circuit has been fabricated using Vitesse Semiconductor 0.6 µm E/D-MESFET process designed for digital VLSI circuits [5]. The process did not support inductors, and the capacitors built from three wiring layers had small capacitance per unit area and large parasitics to substrate. The active circuit area is 1050 µm x 500 µm including 77 transistors.

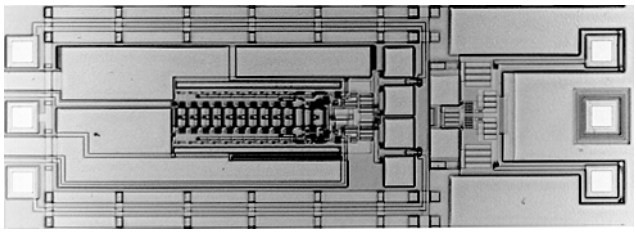

Fig. 5. Microphotograph of the chip

MEASURED RESULTS

The circuit met the design objectives of 2 GHz input bandwidth with small conversion loss, and the measurements matched well with the simulations. We measured the circuit with two different LO-frequencies of 500 MHz and 100 MHz. The results are summarized in Table 1. The input response to a fixed IF is shown in Fig. 6. The notch at 2 GHz is due to the imperfections of the probe card used in measurements. Fig. 7 shows the harmonic characteristics of the circuit.

The circuit can operate with a large range of sampling frequencies from 40 MHz to 1.5 GHz, and the minimum required LO input power is only -2 dBm. The nominal supply voltage is 3V but the digital supply for the strobe pulse generator can be as low as 2.7 V. The strobe pulse generator dissipates 125 mW of power which is much lower than in some earlier diode bridge samplers [8],[9]. The output buffer needs to drive 50Ω loads, and therefore consumes 102 mW. For an on-chip load the dissipation would be significantly smaller.

f_{LO}	500 MHz	100 MHz
RF Input Bandwidth	2.0 GHz	1.6 GHz
System Gain	3 dB	2 dB
Sampler Gain	-1 dB*	-2 dB*
Buffer Gain	4 dB*	4 dB*
Single-Tone		
IIP_3	+16 dBm	+19 dBm
-1dB Compression	+7 dBm	+5 dBm
Two-Tone		
IIP_3	+10 dBm	+10 dBm
-1dB Compression	-1 dBm	-1 dBm
Noise Figure**	23 dB	29 dB

* Estimates based on simulations
** Output buffer noise excluded

Table 1. Measured circuit performance

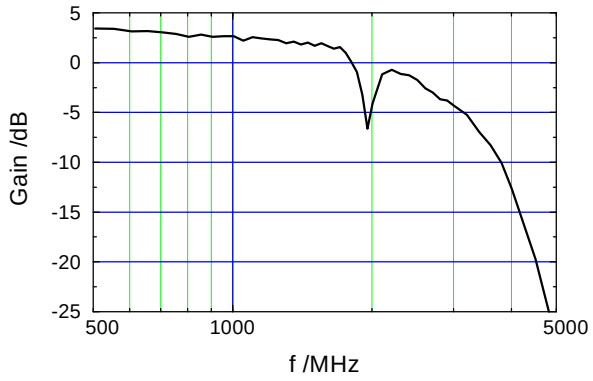

Fig. 6. Input bandwidth of the sampler. The system gain is measured at fixed 5 MHz IF. The sampling frequency is approximately 500 MHz producing the desired IF when RF signal, shown in the x-axis, is varied.

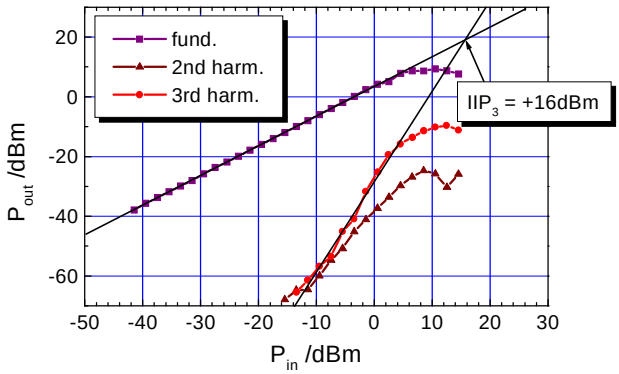

Fig. 7. Harmonic behavior of the circuit in the single-tone measurement. Input signal at 1005 MHz is downconverted with 500 MHz LO giving 5 MHz IF output and its harmonics.

CONCLUSIONS

We have implemented a diode bridge based subharmonic mixer operating at mobile radio frequencies up to 2 GHz. Small conversion loss for a passive mixer (1 dB) has been achieved with high linearity. The circuit operates from a 3 V power supply and dissipates less power than many other diode bridge samplers. Noise aliasing is an inherent problem in subharmonic sampling, but it can be reduced by using high sampling frequencies. Together with other discrete-time analog signal processing and high-speed A/D-conversion techniques, sampling downconversion is a promising choice for new generation receiver architectures.

ACKNOWLEDGMENTS

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